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S. No			Page No.
1.	**Authors:**	**Neha Thombare, Pallavi Deshmukh, Simantini Patil, Shailesh Jain**	
	Paper Title:	**Personalized Image Search**	
	Abstract: Personalized Search is a feature in which when a user is logged into a account, all of his or her searches on Personal Search are recorded into Web History. Then, when a user performs a search, the search results are not only based on the relevancy of each web page to the search term, but the service also takes into account what websites the user previously visited through search results to determine which search results to determine for future searches, to provide a more personalized experience. The feature only takes effect after the user has performed several searches, so that it can be calibrated to the user's tastes. Social sharing websites like facebook, twitter, YouTube they are allowing user to comment, tag, like and unlike the shared documents or images. Rapid Increase in the search services for social websites has been developed. **Keywords:** Personalized Search, Tagging, Topic Model. **References:** 1. Learn to Personalized Image Search from the Photo Sharing Websites Jitao Sang, Changsheng Xu, Senior Member, IEEE, Dongyuan Lu 2. B. Smyth, "A community-based approach to personalizing web search,"Computer, vol. 40, no. 8, pp. 42–50, 2007. 3. Personalized Search on Flickr based on Searcher's Preference Prediction Dongyuan Lu, Qiudan Li	**1-3**
2.	**Authors:**	**Y.Shekar, B. Vasunayak, J. Sunil Kumar, A. Sanyasi Rao, Fathima Shireen**	
	Paper Title:	**Cryptographic Algorithms Implementation on RISC Processor**	
	Abstract: Security is one of the most important features in data communication. Cryptographic algorithms are mainly used for this purpose to obtain confidentiality and integrity of data in communication. Implementing a cryptographic algorithm on a general purpose processor it results lower throughput and larger power consumption. In this work we propose processor architecture to perform the cryptographic algorithms and also it speed up the encryption and decryption process of data. This processor will perform the cryptographic operations as like general instructions in GPP. The data size of this processor is 32-bit. The architecture of the processor designed using Verilog HDL. **Keywords:** Cryptographic Algorithms, GPP, Verilog. **References:** 1. Jun-hong chen "A High-Performance Unified Field Reconfigurable Cryptographic Processor". IEEE-2010 2. Nima Karimpour Darav "CIARP: Crypto Instruction-aware RISC Processor.IEEE-2012" 3. Antonio H. Zavala "RISC-Based Architecture for Computer Hardware Instruction" IEEE-2011 4. "Data Encryption Standard" 1999 october 25. 5. "Advance Encryption Standard" November 26 2001 6. Imyong Lee, Dongwook Lee, Kiyoung choi, "ODALRISC: A Small, Low power and Configurable 32-bit RISC processor," International SOC design Conference 2008. 7. Wayne Wolf, FPGA Based System Design, Prentice Hall, 2005. 8. National Institute of Standards and Technology (NIST), "Advanced Encryption Standard (AES), (FIPPUB 197)", November 26, 2001, http://csrc.nist.gov/publications/. 9. Atri. Rudra, Pradeep k. Dubey, Charanjit S.Jutla, Vijay Kumar, Josyula R.Rao, Pankaj Rahotgi, "Efficient Implementation of Rijndael Encryption with Composite Field Arithmetic," Proceedings of Cryptographic Hardware and Embedded Systems (CHES), Vol. 2162, pp.175-188, 2001. 10. Rohit Sharma, Vivek Kumar Sehgal, Nitin Nitin1, Pranav Bhasker, Ishita Verma, "Design and Implementation of 64-Bit RISC Processor using Computer Modeling and Simulation," Proceedings of UKsim, Vol. 11, pp. 568 – 573, 2009. 11. R. Uma, "Design and performance analysis of 8-bit RISC Processor using Xilinx tool," International Journal of Engineering Research and Applications (IJERA), Vol. 2, Issue 2, pp.53-58, March-April 2012, ISSN: 2248-9622. 12. Jean-Luc Beuchat, "FPGA Implementations of the RC6 Block Cipher,'' Laboratoire de l'Informatique du arall´elisme, Ecole Normale Sup´erieure de Lyon,46, All´ee d'Italie, F–69364 Lyon Cedex 07. 13. Arturo Diaz-Perez, Nazar A. Saqib, Francisco Rodriguez-Henriquez, ''Implementing Symmetric-Key Cryptosystems on Reconfigurable-Hardware,'' springer Nov 2006, ISBN : 0387338837. 14. Imyong Lee, Dongwook Lee, Kiyoung choi, "ODALRISC: A Small, Low power and Configurable 32-bit RISC processor," International SOC design Conference 2008. 15. R. Razdan and M.D. Smith, "A High-Performance Micro architecture with Hardware-Programmable Functional Units," Proceedings of. Micro-27, pp. 172-180, 1994. 16. Vincent P. Heuring, and Harry F. Jordan, "Computer Systems Design and Architecture," Second Edition, 6th Dec, 2003, ISBN-10: 0130484407. 17. Dave Van den Bout "The Practical XILINX Designer Lab Book," pp.30-31, ISBN 0-13- 095502-7. 18. XILINX datasheet library, http:// www.xilinx.com/ partinfo/4000.pdf 19. Jonas Thor, "Evaluation of a reconfigurable computing engine for digital communication Applications," pp.12-17, ISSN 1402-1617. 20. Rasset T.L, Niederland R.A, Lane J.H, Geideman W.A "A 32-b RISC Implemented in Enhancement-Mode JFET Ga As," Vol.3, pp.60-70, 9 Oct 1986. 21. Dolle.M, Jhand. S, Lehner.W, Muller.O, Schlett.M. "A 32-b RISC/DSP microprocessor with reduced complexity," Proceedings of journals and magazines, Vol. 32, Issue 7, pp 1056-1066, 06 August 2002. 22. Buhler, M. Baitinger "VHDL-based development of a 32-bit pipelined RISC processor," U.G. Stuttgart University, Vol 1, pp. 138-142, 06 August 2002.	**4-8**
	Authors:	**Geethanjali Marri, P. Sri Padma, Ch. Ganapathi Reddy**	
	Paper Title:	**Conjugate Gradient Based MMSE Filter for Uplink Orthogonal Frequency Division Multiple Access Systems**	

3.

Abstract: Carrier Frequency Offset (CFO) compensation is very important for reliable detection of transmitted data in uplink Orthogonal Frequency Division Multiple Access (OFDMA) systems. In this paper we proposed a low-complexity CFO compensation algorithm based on the Minimum Mean Square Error (MMSE) criterion for uplink OFDMA systems. The proposed algoritm employs a Conjugate Gradient (CG) method which iteratively finds the MMSE solution. In this paper we are presenting the proposed method by comparing with the existing direct MMSE method and we show that CFO can be compensated with substantially reduced computational complexity by applying the CG method.

Keywords: Carrier Frequency Offset (CFO), Orthogonal Frequency Division Multiple Access (OFDMA), Conjugate Gradient (CG).

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4.

Authors:	**Sreenivasa Reddy Mula**
Paper Title:	**Power Factor Correction**

Abstract: In this paper, a new parallel-connected single phase power factor correction (PFC) topology using flyback converter in parallel with forward converter is proposed to improve the input power factor with simultaneously output voltage regulation taking consideration of current harmonic norms. Paralleling of converter modules is a well-known technique that is often used in medium-power applications to achieve the desired output power by using smaller size of high frequency transformers and inductors. The proposed approach offers cost effective, compact and efficient AC-DC converter by the use of parallel power processing.Forward converter primarily regulates output voltage with fast dynamic response and it acts as master which processes 60% of the power. Flyback converter with AC/DC PFC stage regulates input current shaping and PFC, and processes the remaining 40% of the power as a slave. A parallel-connected interleaved structure offers smaller passive components, less loss even in continuous conduction inductor current mode, and reduced volt-ampere rating of DC/DC stage converter. MATLAB/SIMULINK is used for implementation and simulation results show the performance improvement.

Keywords: Ac-dc converter, pwm, pfc, simulink, matlab.

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Authors:	**Raghava Yathiraju**
Paper Title:	**Acoustic Echo Cancellation Using Conventional Adaptive Algorithms**

Abstract: An adaptive filter is a filter that self-adjusts its transfer function according to an optimization algorithm driven by an error signal.Because of the complexity of the optimization algorithms,most adaptive filters are digital filters.Adaptive filtering constitutes one of the core technologies in digital signal processing and finds numerous application areas in science as well as in industry. Adaptive filtering techniques are used in a wide range of applications, including, adaptive noise cancellation, echo cancellation, adaptive equalization and adaptive beamforming. Acoustic echo cancellation is a common occurrence in today's telecommunication systems. The signal interference caused by acoustic echo is distracting to users and causes a reduction in the quality of the communication. This paper focuses on the use of Least Mean Square (LMS), Normalised Least Mean Square (NLMS), Variable Step-Size Least Mean Square (VSLMS), Variable Step-Size Normalised Least Mean Square (VSNLMS) and Recursive Least Square (RLS) algorithms to reduce this unwanted echo, thus increasing communication quality.

Keywords: Adaptive filters, Echo, Adaptive algorithms, Echo cancellation, Acoustic echo cancellation.

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5. **18-24**

6. **25-29**

Authors:	**Omar Turath Tawfeeq**
Paper Title:	**THD Reduction of A Current Source Rectifier-DC Motor Drive Using Single Tuned Filters**

Abstract: A current source rectifier (CSR) is commonly used to supply a DC Motor with variable voltage for variable speed applications. A study of THD Reduction using single tuned filters employed to obtain the required low harmonic distortion and nearly unity power factor in A.C supply current over a wide range of operating shaft speed. The external performances of a three-phase CSR-fed separately excited DC motor drive such as power factor, harmonics factor, and efficiency using sinusoidal pulse width modulation (SPWM) control technique are obtained for different speeds and modulation indexes. Separately excited DC motors with armature voltage control provides constant torque operation. The effectiveness of the proposed system (2.3-kW 13A DC motor drive) was verified through computer Matlab simulations.

Keywords: Current source rectifier, DC Drive, THD Reduction, Single tuned filters, SPWM.

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7.

Authors: Sainath A. Waghmare, Chandan D. Chaudhari, Sumit N. Gavande

Paper Title: Numerical Analysis and Experimental Failure Mode Determination of Composite T -Joint

Abstract: The use of fibre composite materials in more demanding roles is increasing due to increased performance requirements in various applications. One type of joint in a sandwich panels in superstructure is a T-joint. An existing design consists of panels joined by filler material and overlaminates of the same thickness as the skin laminates. The aim of the research was to determine the methodology to predict the failure mode of the T-Joint under a pull-off tensile loading using Finite Element model. The outcome of the research was that the Finite Element (FE) simulations were used in conjunction to determine the failure mechanism of the T-Joint in the presence of disbonds in the critical location. Stress distributions are investigated by both laboratory tests and numerical modeling, and design criteria for core pieces are presented.

Keywords: Sandwich panels, Overlaminates, T-joint, Core pieces, FRP.

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8.

Authors: Kushal M. L, V. Venkateswarlu

Paper Title: Design and Implementation of Phase Modulation Using PLL for Polar Transmitter

Abstract: In this paper the phase modulation of polar transmitter has been implemented. The circuit for implementing phase modulation consists of Phase Lock Loop (PLL), Sigma Delta Modulator (SDM) and differentiator. The input signal is applied at the differentiator which will convert phase component to the frequency of the signal. The obtained frequency signal is given to the SDM which will convert the analog signal to the digital signals. The SDM should have four bits of resolution, equivalently 36 dB signal-to-noise-and-distortion-ratio (SNDR) for a 200 kHz bandwidth. For supply voltages from 2.5 V to 3 V, the current supply is desired to be less than 20 mA. The PLL consists of the reference signal of 125MHz, and output voltage around 2-3GHz with the VCO gain of 0.277GHz/V. The circuit of PLL, SDM and differentiator are implemented on the Cadence Virtuoso platform.

Keywords: Polar transmitter, phase modulation, Phase lock loop, Sigma delta modulator, differentiator.

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Paper Title: **Self Automated Tool in Vehicular System That Identifies the Air Pollution and the Future of E-Governs**

Abstract: Air pollution is a major issue that we face today. Pollution zone in during earlier century was low but keeps growing towards the current. Studies revealed the fact the concentration in organic and inorganic toxic elements keeps growing depending upon the region and vehicle type. There is a growing demand for the environmental pollution monitoring and control systems. Gas sensors help to detect gas molecules and the concentration of the gas analytical methods of identifying the gases has greater disadvantage than with fairly accurate and selective gas reading.

Keywords: Embedded control, Monitoring system, Remote monitoring, sensor.

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